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DataTap-10 Software Release Notes

March 11, 2020

Note: Each software release can only be used with the listed FPGA revisions. If a release is loaded into a DataTap-10 containing an unsupported FPGA revision, please contact ICS or revert to the files on the CD delivered with the DataTap-10 in order to restore the unit. In this case, the mb0.srd and mb1.srd files must be written directly onto the microSD card with a card reader. See the DataTap-10 User's Manual for FPGA revision history.

For further information or questions contact:

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Release 11-Mar-2020:

Software Revision Numbers
==========

CPU 0: Mar 11 2020 22:06:03
CPU 1: Mar 11 2020 22:06:12

Applicable FPGA revisions
==========

- 12091901
- 05231701
- 12091601
- 06141601
- 12291501
- 09141501
- 01061501
- 09031401
- 05121401
- 04231401
- 08301301

Modifications
==========

- Added the parameter "NUM_UDP_STS_MSGS" to the system configuration file to allow up to 3 status messages to be sent out of the DataTap-10 with successive destination port numbers every ASCB frame. The addition of this parameter brings the version up to 1.16 for the system configuration file. Note that the UDP destination port of the first status message is UDP_HOST_PORT_STS and it increments by 1 for each status message specified to be sent out. Also note that UDP_STS_EN_DEF must be set to TRUE to allow any UDP status messages to be sent out.

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Release 10-Feb-2020:

Software Revision Numbers
==========

CPU 0: Feb 10 2020 20:31:49
CPU 1: Feb 10 2020 20:31:59

Applicable FPGA revisions
==========

- 12091901
- 05231701
- 12091601
- 06141601
- 12291501
- 09141501
- 01061501
- 09031401
- 05121401
- 04231401
- 08301301

Modifications
==========

- Added a bit in the extended status field of the UDP Status Messages to indicate when the DataTap-10 is in eASCB-MAX mode.

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Release 18-Dec-2019:

Software Revision Numbers
==========

CPU 0: Dec 18 2019 22:24:22
CPU 1: Dec 18 2019 22:24:32

Applicable FPGA revisions
==========

- 12091901
- 05231701
- 12091601
- 06141601
- 12291501
- 09141501
- 01061501
- 09031401
- 05121401
- 04231401
- 08301301

Modifications
==========

- Added support for eASCB-MAX.
- Added the allowable value of "eASCB-MAX" to the "ASCB_VERSION" parameter in the system configuration file, bumping the file version up to 1.15.
- Added the allowable parameters "ASCB_RX_BUF_SIZE" and "ASCB_TX_BUF_SIZE" to the system configuration to allow changing of the ASCB buffer sizes for eASCB-MAX. The default values are 6144 for transmit and 15360 for receive.

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Release 10-Oct-2017:

Software Revision Numbers
==========

CPU 0: Oct 10 2017 20:42:55
CPU 1: Oct 10 2017 20:43:03

Applicable FPGA revisions
==========

- 05231701
- 12091601
- 06141601
- 12291501
- 09141501
- 01061501
- 09031401
- 05121401
- 04231401
- 08301301

Modifications
==========

- Made a bug fix for production testing only.

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Release 7-Aug-2017:

Software Revision Numbers
==========

CPU 0: Aug 7 2017 21:52:01
CPU 1: Aug 7 2017 21:52:09

Applicable FPGA revisions
==========

- 05231701
- 12091601
- 06141601
- 12291501
- 09141501
- 01061501
- 09031401
- 05121401
- 04231401
- 08301301

Modifications
==========

- Added decoding of ASCB-C parameters based on the tis.cfg file loaded on the microSD card. The decoded parameters are sent out over UDP and are displayed over Telnet. The tis.cfg file for ASCB-C can be created with FlightLine v14.0 and later. Note that the ASCB-C receive logic is only available in FPGA revision 01061501 and later.

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Release 25-May-2017:

Software Revision Numbers
==========

CPU 0: May 25 2017 22:03:06
CPU 1: May 25 2017 22:03:14

Applicable FPGA revisions
==========

- 05231701
- 12091601
- 06141601
- 12291501
- 09141501
- 01061501
- 09031401
- 05121401
- 04231401
- 08301301

Modifications
==========

- Made the necessary changes to support a 5MB Consume ESCAPE registry, which is only supported in FPGA revision 05231701 and later. If the Consume ESCAPE registry is larger than the old maximum size of 4MB, the file header for raw recordings in TISNATIVE mode will grow by 1MB to allow registries of up to 5MB. In this case, an ASCII tag of "ESCPE5MB" will exist starting at byte location 8 of the file header. Note that this only applies to the first segment of a recording. If the registry is less than or equal to 4MB, then there is no change to the legacy raw recording format.

  Below is a hex dump of the first 64 bytes of the first segment of a recording where the registry is larger than 4MB:

```
0000000000: 00 00 00 00 00 00 00 00 45 53 43 50 45 35 4D 42   ........ESCPE5MB
0000000010: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
0000000020: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
0000000030: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
```

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Release 16-Jan-2017:

Software Revision Numbers
==========

CPU 0: Jan 16 2017 21:18:38
CPU 1: Jan 16 2017 21:18:45

Applicable FPGA revisions
==========

- 12091601
- 06141601
- 12291501
- 09141501
- 01061501
- 09031401
- 05121401
- 04231401
- 08301301

Modifications
==========

- Added the parameter "ASCBC_FRAME_SIZE" to the system configuration file parsing code to allow ASCB-C frames sent out over UDP to be truncated to the specified value. This parameter will not be listed in the default system configuration file, so the configuration file revision was not bumped, but it will remain a usable parameter in all future releases. Valid values are anywhere between 1 and 2048 bytes. Note that it does not affect the size of the frames being recorded to the microSD or optional CompactFlash card as those will always be 2048 bytes.

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Release 12-Jan-2017:

Software Revision Numbers
==========

CPU 0: Jan 12 2017 19:23:26
CPU 1: Jan 12 2017 19:23:35

Applicable FPGA revisions
==========

- 12091601
- 06141601
- 12291501
- 09141501
- 01061501
- 09031401
- 05121401
- 04231401
- 08301301

Modifications
==========

- Added the parameter "REC_MAX_SEG_SIZE_MB" to the system configuration file to allow specifying of the maximum file segment size used during recording. A new recording file segment will be opened once the specified size has been reached. This applies to all recording types (ASCB, ARINC-429, and ARINC-717). Any power of 2 value between 16 and 2048 (MB) can be specified, with the default and legacy value being 2048 (2GB). Note that the smaller the value, the higher the chance of a recording overflow occurring due to the increased number of files generated. The DataTap-10 software must parse through all existing filenames when a new file is opened, which consumes more CPU time as the number of files grows. This can lead to an overflow condition due to the limited buffering on the DataTap-10. If an overflow condition does occur, only full frames of data are dropped such that the integrity of the recording remains intact.
- Bumped the system configuration file version up to 1.14 due to the addition of the "REC_MAX_SEG_SIZE_MB" parameter.

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Release 13-Dec-2016:

Software Revision Numbers
==========

CPU 0: Dec 13 2016 21:32:22
CPU 1: Dec 13 2016 21:32:29

Applicable FPGA revisions
==========

- 12091601
- 06141601
- 12291501
- 09141501
- 01061501
- 09031401
- 05121401
- 04231401
- 08301301

Modifications
==========

- Added software support for ASCB-A.
- Added the ability to set the system time using a UDP Command Input Datagram. This command will initialize the internal Precision Time Protocol (IEEE-1588v2) clock to the specified value. Note that "USE_TIMING_SOURCE" must be set to "IEEE-1588v2" in the system configuration file in order for the time to be used as the system time.
- Added the parameter "REC_STOP_NO_ASCB" to the system configuration file to allow any active recordings to be automatically stopped when no ASCB data is present.
- Bumped the system configuration file version up to 1.13.
- Modified the names of the following parameters in the system configuration file to clarify that they apply to all recording types rather than just ASCB. Note that the previous parameter names can still be used in order to maintain compatibility with older configuration files.
    - ASCB_REC_APPEND is now REC_APPEND_MODE
    - ASCB_CIRC_REC_MODE is now CIRC_REC_MODE
    - ASCB_REC_WAIT_DATA is now AUTO_REC_WAIT_ASCB

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Release 25-Oct-2016:

Software Revision Numbers
==========

CPU 0: Oct 25 2016 11:54:16
CPU 1: Oct 25 2016 11:54:26

Applicable FPGA revisions
==========

- 06141601
- 12291501
- 09141501
- 01061501
- 09031401
- 05121401
- 04231401
- 08301301

Modifications
==========

- Fixed a bug which prevented playback from being automatically started on power-up in certain cases. Note that playback on power-up occurs when the PLAYBACK_MODE parameter in the system configuration file is set to RXRAW or TXRAW and the desired playback file is specified with the PLAYBACK_FILE parameter.

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Release 28-Jul-2016:

Software Revision Numbers
==========

CPU 0: Jul 28 2016 08:09:10
CPU 1: Jul 28 2016 08:09:21

Applicable FPGA revisions
==========

- 06141601
- 12291501
- 09141501
- 01061501
- 09031401
- 05121401
- 04231401
- 08301301

Modifications
==========

- Added the Host Tx Playback Mode which allows playback onto the ASCB bus from a recorded file set using FlightLine. The entire ASCB bus is reproduced with the exact timing and data as when the recording was taken. This mode is similar to the Tx Raw Playback Mode, but the recording file set resides on the host PC rather than the DataTap-10's microSD or CompactFlash card. This prevents the user from having to copy recordings to the DataTap-10's media card, which can be time-consuming. Note that FlightLine monitors the occupancy of the DataTap-10's large internal playback buffer and aims to keep it half-full. This eliminates the need for FlightLine to have to send the data in real-time, making it much more robust.
- Added bits to the Status UDP Output Datagrams to indicate when the DataTap-10 is in Host Tx Playback Mode as well as when the playback buffer is half-full.
- Fixed a bug in the 17-Jun-2016 release which affected only the 05121401 and 04231401 FPGA versions and prevented proper synchronization to the ASCB bus in certain cases.

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Release 17-Jun-2016:

Software Revision Numbers
==========

CPU 0: Jun 17 2016 16:35:25
CPU 1: Jun 17 2016 16:35:36

Applicable FPGA revisions
==========

- 06141601
- 12291501
- 09141501
- 01061501
- 09031401
- ~~05121401~~
- ~~04231401~~
- 08301301

Modifications
==========

- Moved the software stack of both processors into Block RAM to significantly reduce the number of accesses to local memory, leaving more bandwidth for the hardware modules. As a result, 8192 parameters can now be fully supported by the decode engine under most, if not all, conditions. The encode engine may still not be able to support the full 8192 parameters depending on the number of floats to be encoded (i.e. if greater than several thousand). This is due to the length of time it takes to encode a float parameter for transmission onto the ASCB bus. Note that the DataTap-10 can support 8192 total parameters (encode + decode), and this may be split between encode and decode in any desired fashion using the TIS configuration files.
- Optimized the multi-stream recording by forcing only full clusters of data to be written to the media card. This leads to recording in a very linear fashion and may allow a wider variety of microSD card brands to be used in the future. The Samsung PRO and PRO+ are still the recommended microSD cards to use, however, as they outperform all other brands and models.
- Added the parameter "STS_LED_USE" to the system configuration file, which supersedes "USE_STS_LED_FOR_REC_STS". The new parameter allows additional options to be specified which can force the Status LED to green or off after a successful initialization. This is useful in stand-alone configurations by preventing the LED from going to static red due to no connection to FlightLine.
- Added software to support the interrupt coalescing timers for the ARINC-429, ARINC-717, and ASCB-C receive modules, significantly reducing CPU usage.
- Modified the IEEE1588v2 software to support fine-tuning of the master offset in hardware rather than making adjustments in software. This leads to a much more accurate implementation, as can be verified using discrete output 1 when configured for PPS.
- Added the following parameters to the system configuration file, bumping the file revision up to 1.12:
    - STS_LED_USE

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Release 12-Feb-2016:

Software Revision Numbers
==========

CPU 0: Feb 12 2016 11:13:19
CPU 1: Feb 12 2016 11:13:35

Applicable FPGA revisions
==========

- 12291501
- 09141501
- 01061501
- 09031401
- 05121401
- 04231401
- 08301301

Modifications
==========

- Added the state of all 4 discrete inputs into the ASCB raw recordings to allow them to be used for event marking. Note that a given discrete input must be stable for 100 milliseconds before a state change is recognized. The raw recording structures changed as shown below in red and will be reflected in revision R of the DataTap-10 User's Manual:

    - Enhanced-ASCB/ASCB-D Raw Recording Structure

```
typedef struct
{
   uint32 frame_tick;       // ASCB Frame Number
   uint32 discretes;        // [31:4]=RFU, [3:0]=Disc Inputs 4:1
   uint32 unused1;          // RFU
   uint32 unused2;          // RFU
   uint32 IRIG1;            // IRIG Time 1
   uint32 IRIG2;            // IRIG Time 2
   uint32 IRIG3;            // IRIG Time 3
   uint32 IRIG4;            // IRIG Time 4
   char   format_str[8];    // Format String - always "eASCB   " to indicate full-size
                            // frames are being recorded, even for ASCB-D.
   uint08 unused3[472];     // RFU

   uint08 rx2_data[0x3000]; // RX2 Raw NIC Frame Buffer Data
   uint08 rx1_data[0x3000]; // RX1 Raw NIC Frame Buffer Data

} record_block_t;
```

    - ASCB-C Raw Recording Header Structure

```
typedef struct
{
   uint32 status;           // [31:28]=Disc Inputs 4:1, [27:1]=RFU, [0]=Bus
   uint32 timestamp;        // Value of 20 nsec system counter
   uint32 count;            // Count of frames recorded
   uint32 size;             // Frame Size - always 2048 (excludes rec header)

} ascbc_rec_hdr_t;
```

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Release 04-Feb-2016:

Software Revision Numbers
==========

CPU 0: Feb 4 2016 12:41:06
CPU 1: Feb 4 2016 12:41:29

Applicable FPGA revisions
==========

- 12291501
- 09141501
- 01061501
- 09031401
- 05121401
- 04231401
- 08301301

Modifications
==========

- Added the ability to record ASCB, ARINC-429, and ARINC-717 simultaneously. Note that only the Samsung PRO 64GB microSD cards and the SanDisk Extreme Pro CompactFlash cards are supported for this functionality. For microSD only, the DataTap-10 MUST be used for formatting the card (via the FTP server) when recording multiple data streams. The formatting process using the DataTap-10 is automated in FlightLine via the "Format Media" button.
- Added the ability to play back a recording file set onto the ASCB bus rather than just over UDP. In this case, the DataTap-10 will act as all NIC IDs and transmit all data onto the bus, mimicking the entire ASCB bus with the exact data and timing from when the recording was taken. Note that the DataTap-10 must have the transmission hardware option installed in order to use this feature. Whether to play back over ASCB or UDP is configured in the system configuration file using the values TXRAW or RXRAW, respectively, for the existing PLAYBACK_MODE parameter. Alternatively, FlightLine (v12.10 or later) can be used to start either playback mode, and will automatically retrieve a list of available recording files from the DataTap-10.
- Added four fields to the Telnet screens and UDP Status Output datagrams to allow monitoring of the DataTap-10's parameter encode and decode engines. Depending on the amount of data being received on the ARINC-429 busses, less than 8192 total ASCB parameters (encode + decode) may be supported, especially if ASCB recording is active. The parameter encode and decode engines must complete within one ASCB frame (12.5 milliseconds) or data corruption or parameter group status errors can inadvertently be generated. The added fields indicate the percentage load of each engine and the number of times each engine has exceeded the ASCB frame time. As such, the number of parameters in any of the TIS configuration files loaded onto the DataTap-10's microSD card should be reduced until the counts are no longer incrementing and the peak loads stay below 100%. These fields are displayed in FlightLine v12.10 or later on the DataTap-10 Performance Monitor Form. Note that the encode engine is only used when the hardware transmit PDD is enabled (i.e. HW_TX_PDD_ENABLE set to TRUE).
- Added edge-triggered discrete input recording control. Edge-triggered control allows recording control via Telnet, UDP, and FlightLine to be used as well, whereas the existing level-sensitive control does not.
- Added the parameter A717_INPUT to the system configuration file. This allows control over an 8-input mux added in FPGA revision 12291501 for the ARINC-717 input, allowing any discrete input or ARINC-429 receive channel to be used for ARINC-717. Note that the maximum supported word rate when using a discrete input is 512 wps, whereas for an ARINC-429 channel it can go up to 8192 wps.

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- Added parameters A429_RX[1:4]_CONFIG to the system configuration file to allow configuration of the ARINC-429 receive channels (LOW, HIGH, or OFF) on power-up. If ARINC-429 recording is enabled at power-up, these parameters must be used to determine the configuration of each channel.
- Added parameter AUTO_REC_ENABLE to the system configuration file. This parameter was added to allow manual recording control (i.e. via a discrete input) using the RAW_REC_EN, DEC_REC_EN, A429_REC_EN, and A717_REC_EN parameters. In earlier versions, setting any of these parameters to TRUE would force recording to begin at power-up. Setting AUTO_REC_ENABLE to FALSE will prevent automatic recording at power-up. The default value is TRUE to maintain compatibility with older configuration files.
- Added parameters UDP_A429_EN_DEF and UDP_A717_EN_DEF to allow default control over sending out of UDP datagrams when ARINC-429 and ARINC-717 data is received, respectively. These values default to TRUE, but should be set to FALSE if these interfaces are being used but no UDP output is required.
- Added the following parameters to the system configuration file, bumping the file revision up to 1.11:
    - A429_REC_EN
    - A717_REC_EN
    - UDP_A429_EN_DEF
    - UDP_A717_EN_DEF
    - AUTO_REC_ENABLE
    - A429_RX1_CONFIG
    - A429_RX2_CONFIG
    - A429_RX3_CONFIG
    - A429_RX4_CONFIG
    - A717_INPUT

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Release 04-Nov-2015:

Software Revision Numbers
==========

CPU 0: Nov 4 2015 15:54:20
CPU 1: Nov 4 2015 15:54:41

Applicable FPGA revisions
==========

- 09141501
- 01061501
- 09031401
- 05121401
- 04231401
- 08301301

Modifications
==========

- Changed the memory alignment of the decoded datagrams such that the portions updated by software and the portions updated by hardware exist on separate cachelines. In previous software versions, old data could inadvertently be sent out in the first few channels of each decoded datagram due to cacheline flushing under certain conditions.

Note: This software release can only be used with the listed FPGA revisions. See the DataTap-10 User's Manual for FPGA revision history.

Release 15-Sept-2015:

Software Revision Numbers
==========

CPU 0: Sep 15 2015 14:26:04
CPU 1: Sep 15 2015 14:26:22

Applicable FPGA revisions
==========

- 09141501
- 01061501
- 09031401
- 05121401
- 04231401
- 08301301

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Modifications
==========

- Added Circular Recording mode.
- Added Record Append mode.
- Added ARINC-717 recording.
- Added recording control via the discrete inputs.
- Added the command "quote site fill" to the FTP server to fill the media card with empty 2GB files for use with Circular Recording Mode.
- Added the command "quote site full format" to the FTP server to allow erase commands to be issued to the entire microSD card prior to creating the FAT32 partition. The erasing adds between 10 to 30 seconds (depending on its current state) to the format time of a Samsung 64GB PRO microSD card, but greatly improves recording performance and extends the life of the card.
- Added to the FTP format commands the actual creation of a FAT32 file system on the selected media type (microSD or CompactFlash). The commands now overwrite the existing file system and create a FAT32 file system.
- Added the ability to wait a configurable period of time after power-up before starting automatic recording.
- Added the ability to wait for ASCB traffic to be present prior to starting an automatic recording from power-up.
- Added software compatibility with FPGA revision 08301301.
- Added several fields to the Status Output Datagrams to allow monitoring of potential performance degradation of the recording media over time.
- Added the following parameters to the system configuration file, bumping the file revision up to 1.10:
    - ASCB_REC_APPEND
    - ASCB_CIRC_REC_MODE
    - ASCB_REC_WAIT_DATA
    - AUTO_REC_DELAY_SEC
    - DIN1_CONFIG
    - DIN2_CONFIG
    - DIN3_CONFIG
    - DIN4_CONFIG

Note: This software release can only be used with the listed FPGA revisions. See the DataTap-10 User's Manual for FPGA revision history.

Release 9-Sept-2015:

Software Revision Numbers
==========

CPU 0: Sep 9 2015 15:58:29
CPU 1: Sep 9 2015 15:58:37

Applicable FPGA revisions
==========

- 01061501
- 09031401
- 05121401
- 04231401

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Modifications
==========

- Added a software work-around to account for a bug in the IRIG logic in all FPGA revisions prior to 09031401. The bug caused the IRIG time to rollover to 00:00:00 from 17:59:59 and to increment to 24:00:00 from 23:59:59. The condition would last for one full second until the next IRIG frame was received and would correct the time. The logic bug was fixed in FPGA revision 09031401.
- Fixed an issue introduced into version 10-Feb-2015 where the registry written into the .01 file when recording with the DataTap-10 may be byte-swapped. This only applies to FPGA revisions 05121401 and 04231401 and can be worked around by specifying the registry rather than using the recorded registry when playing back a file with FlightLine.

Note: This software release can only be used with FPGA revisions 01061501, 09031401, 05121401, or 04231401. See the DataTap-10 User's Manual for FPGA revision history.

Note: A separate software release on Sept 9, 2015 also exists for FPGA revisions 07241301 and 10301201. Please see the sections below for details on that release.

Release 17-Jun-2015:

Software Revision Numbers
==========

CPU 0: Jun 17 2015 16:22:56
CPU 1: Jun 17 2015 16:23:09

Applicable FPGA revisions
==========

- 01061501
- 09031401
- 05121401
- 04231401

Modifications
==========

- Added the option TMG_MSG_STRING to the system configuration file to allow specifying of the string embedded in timing messages sent from the DataTap-10 when configured for transmission as a timing NIC.
- Added printing of the string embedded in each received timing message to the "NIC Status Page" available over Telnet.
- Bumped the system configuration file version to 1.9 as a result of modifying it for the changes listed in this release.

Note: This software release can only be used with FPGA revisions 01061501, 09031401, 05121401, or 04231401. See the DataTap-10 User's Manual for FPGA revision history.

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Release 10-Feb-2015:

Software Revision Numbers
==========

CPU 0: Feb 10 2015 13:01:29
CPU 1: Feb 10 2015 13:01:36

Applicable FPGA revisions
==========

- 01061501
- 09031401
- 05121401
- 04231401

Modifications
==========

- Added support for ASCB-C playback over UDP.
- Fixed an issue where an FTP read transfer terminates due to running out of memory in the rare case a Maximum Transfer Unit is not specified by the host computer during the TCP data connection set-up.
- Significantly improved the speed of all FTP transfers.
- Added a bit to the status field of the status output messages to indicate when the DataTap-10 is in the hardware PDD transmission mode for ASCB-D and eASCB.
- Changed the default for ASCB_FLOAT_ENCODE_MODE to rounding rather than truncation such that the output will match that of earlier DataTap-10 FPGA versions.
- Bumped the system configuration file version to 1.8 as a result of modifying it for the changes listed in this release.

Note: This software release can only be used with FPGA revisions 01061501, 09031401, 05121401, or 04231401. See the DataTap-10 User's Manual for FPGA revision history.

Release 15-Jan-2015:

Software Revision Numbers
==========

CPU 0: Jan 15 2015 16:04:35
CPU 1: Jan 15 2015 16:04:45

Applicable FPGA revisions
==========

- 01061501
- 09031401
- 05121401
- 04231401

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Modifications
==========

- Added software support for ASCB version C, which includes sending out received ASCB-C data in UDP datagrams and recording to microSD or CompactFlash. This functionality is only available in FPGA revision 01061501 or later.
- Added an indication using the 8 front LEDs to indicate when the DataTap-10 is currently playing back a recording over UDP. The LEDs will continuously move from side-to-side in top/bottom pairs.
- Added the following to the system configuration file, which bumps the configuration file version to 1.7:
    - **ASCB_VERSION** – This supersedes the ENHANCED_ASCB_MODE parameter. Either can be used, but only ASCB_VERSION can be used to indicate ASCB version C. Both should not be included in the same configuration file.
    - **ASCB_FLOAT_ENCODE_MODE** – This allows floating point values to be either truncated or rounded when converted to integers as part of the encoding process for transmission onto the ASCB bus. Previous mode was always to round, but additional logic was created to allow truncation in order to match Honeywell TIU output. This functionality is only available in FPGA revision 01061501 or later.
    - Allowed all parameters containing the word "FULL_" to be replaced with "RAW_" and the word "PARTIAL_" to be replaced with "DEC_" to match traditional DataTap-10 nomenclature. Either can be used in all cases.

Note: This software release can only be used with FPGA revisions 01061501, 09031401, 05121401, or 04231401. See the DataTap-10 User's Manual for FPGA revision history.

Release 26-Nov-2014:

Software Revision Numbers
==========

CPU 0: Nov 26 2014 11:03:54
CPU 1: Nov 26 2014 11:04:01

Applicable FPGA revisions
==========

- 09031401
- 05121401
- 04231401

Modifications
==========

- Made the necessary changes to allow the latest software to be backwards-compatible with FPGA revisions 05121401 and 04231401.
- Added Passive FTP support. Passive mode, if supported by the host, prevents potential blocking of the FTP data connection by the host firewall. This was tested using the FTP clients of Windows Explorer, several browsers (Internet Explorer, Mozilla FireFox, and Google Chrome), and Debian Linux. Note that using Windows Explorer as an FTP client (e.g. use ftp://192.168.1.1 to connect to the DataTap-10), allows transferring files to and from the microSD card using simple copy-and-paste commands.

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Note: This software release can only be used with FPGA revisions 09031401, 05121401, or 04231401. See the DataTap-10 User's Manual for FPGA revision history.

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Releases for FPGA Revision 09031401

Release 12-Nov-2014:

Software Revision Numbers
==========

CPU 0: Nov 12 2014 10:50:42
CPU 1: Nov 12 2014 10:50:50

- Fixed a bug where the IRIG year was not always being used for the recording filename and file date/time even though it was specified as non-zero in the system configuration file and the IRIG time was synchronized.
- Made a change to allow any printable characters to be used in the recording filename base specified by PARTIAL_REC_FILE and FULL_REC_FILE, with the exception of the following characters: / \ : * ? " < > |. The exclusions match that of Windows. Note that when one of these excluded characters or a period is encountered, the filename will be truncated at that point and a .01 extension added.

Note: This software release can only be used with FPGA revision 09031401.

Release 28-Oct-2014:

Software Revision Numbers
==========

CPU 0: Oct 28 2014 12:09:41
CPU 1: Oct 28 2014 12:09:50

- Changed the method of verifying whether a parameter is produced or not by parsing all output messages in the associated ESCAPE registry at initialization time rather than using the parameter handle and searching the source table. The previous method was not always accurate.
- Changed the double-buffering scheme of the UDP Parameter Input Datagrams to single-buffering. Double-buffering required datagrams to be sent in every ASCB frame to prevent toggling between new and old values.
- Added a 32-bit field to the status output messages for the ASCB status error count. This is the same count which can be viewed on page 1 of the Telnet screens.
- Added a 32-byte field to the status output messages for continuation of the recording filename in case it exceeds the original 32-byte field. Note that both fields are always null-terminated regardless of the actual length of the filename. FlightLine v12.4 and later will use both fields if populated and display the full concatenated filename in the DataTap window while playing back or recording.
- Added a new command to the UDP command packet protocol to allow for clearing of the ASCB status error count.

Note: This software release can only be used with FPGA revision 09031401.

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Release 4-Sep-2014:

Software Revision Numbers
==========

CPU 0: Sep 4 2014 13:28:00
CPU 1: Sep 4 2014 13:28:09

- Initial software revision for FPGA version 09031401.
- Added support for big-endian NIC and PDD registries. Only little-endian has been supported in previous versions of the DataTap-10.
- Moved the periodic reading of ADC values from software into hardware to save significant CPU time.
- Changed the playback functionality to use a dedicated hardware clock rather than borrowing the PTP clock.

Note: This software release can only be used with FPGA revision 09031401.

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Releases for FPGA Revisions 04231401 and 05121401

Release 17-Nov-2014:

Software Revision Numbers
==========

CPU 0: Nov 17 2014 14:17:28
CPU 1: Nov 17 2014 14:17:38

- Added Passive FTP support. Passive mode, if supported by the host, prevents potential blocking of the FTP data connection by the host firewall. This was tested using the FTP clients of Windows Explorer, several browsers (Internet Explorer, Mozilla FireFox, and Google Chrome), and Debian Linux. Note that using Windows Explorer as an FTP client (e.g. use ftp://192.168.1.1 to connect to the DataTap-10), allows transferring files to and from the microSD card using simple copy-and-paste commands.

Note: This software release can only be used with FPGA revisions 04231401 or 05121401.

Release 5-Nov-2014:

Software Revision Numbers
==========

CPU 0: Nov 5 2014 14:54:35
CPU 1: Nov 5 2014 14:54:43

- Fixed a bug where the IRIG year was not always being used for the recording filename and file date/time even though it was specified as non-zero in the system configuration file and the IRIG time was synchronized.
- Made a change to allow any printable characters to be used in the recording filename base specified by PARTIAL_REC_FILE and FULL_REC_FILE, with the exception of the following characters: / \ : * ? " < > |. The exclusions match that of Windows. Note that when one of these excluded characters or a period is encountered, the filename will be truncated at that point and a .01 extension added.

Note: This software release can only be used with FPGA revisions 04231401 or 05121401.

Release 11-Sep-2014:

Software Revision Numbers
==========

CPU 0: Sep 11 2014 13:42:13
CPU 1: Sep 11 2014 13:42:20

- Added a 32-bit field to the status output messages for the ASCB status error count. This is the same count which can be viewed on page 1 of the Telnet screens.
- Added a 32-byte field to the status output messages for continuation of the recording filename in case it exceeds the original 32-byte field. Note that both fields are always null-terminated regardless of the actual length of the filename. FlightLine v12.4 and later will use both fields if populated and display the full concatenated filename in the DataTap window while playing back or recording.

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- Added a new command to the UDP command packet protocol to allow for clearing of the ASCB status error count.

Note: This software release can only be used with FPGA revisions 04231401 or 05121401. **Release 26-Aug-2014:**

Software Revision Numbers
==========

CPU 0: Aug 26 2014 09:38:18
CPU 1: Aug 26 2014 09:38:24

- Added the ability to use the legacy TIS format when creating filenames for recording. This format appends a timestamp to the filename based on the IRIG or PTPv2 time. If the DataTap-10 is configured to record on power-up, it will wait up to 5 seconds for IRIG or 20 seconds for PTPv2 for time synchronization to occur prior to starting the recording.
- Added the functionality to use the IRIG or PTPv2 time to create the file date and time when writing files to the microSD or CompactFlash card via recording or FTP. If the time is not synchronized when the file is created, the DataTap-10 will use the default of 12:00AM 1/1/2000.
- Fixed an issue when starting playback using the CompactFlash card and either not connected to a live ASCB bus or transmitting. This causes the data to be played back at the normal frame tick rate, which the CompactFlash card cannot keep up with using this FPGA load. A new FPGA load is available which changes the Ultra DMA read behavior and allows playback at normal speed.
- Added the following parameters to the system configuration file, which bumps the configuration file version to 1.6:
    - REC_FILENAME_FORMAT
    - IRIG_YEAR

Note: This software release can only be used with FPGA revisions 04231401 or 05121401.

Release 6-Aug-2014:

Software Revision Numbers
==========

CPU 0: Aug 6 2014 12:10:35
CPU 1: Aug 6 2014 12:10:40

- Added the ability to specify an IRIG start time when playing back a raw recorded file. This can be specified in the system configuration file or in FlightLine version 12.1 or later.
- Added a parameter to the system configuration file (UDP_DEC_LEGACY_MODE) to enable legacy mode for UDP decoded parameter output datagrams. Legacy mode ensures all datagrams contain 256 channels of data and status, regardless of how many channels are actually occupied. It also adds the 32-bit CRC field at the end of the datagram, though the field is always zero.
- Added the following parameters to the system configuration file, which bumps the configuration file version to 1.5:
    - UDP_DEC_LEGACY_MODE
    - PLAYBACK_MODE
    - PLAYBACK_FILE
    - PLAYBACK_IRIG

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Note: This software release can only be used with FPGA revisions 04231401 or 05121401.

Release 28-Jul-2014:

Software Revision Numbers
==========

CPU 0: Jul 28 2014 20:14:07
CPU 1: Jul 28 2014 20:14:12

- Added additional fields and status bits to the Status Output datagrams to allow media and recording information to be displayed starting with FlightLine v12.1.
- Added the ability to playback raw recordings from the selected media type. This allows any changeable set of decoded parameters to be viewed from a raw recording through FlightLine or Telnet by simply changing the TIS configuration file in the DataTap-10 and/or FlightLine. Note that playback only affects the UDP output and Telnet screens and does not transmit anything on the ASCB bus.

Note: This software release can only be used with FPGA revisions 04231401 or 05121401.

Release 28-May-2014:

Software Revision Numbers
==========

CPU 0: May 28 2014 12:51:38
CPU 1: May 28 2014 12:51:43

- Added software to allow ASCB and ARINC-429 recording to CompactFlash rather than the microSD card. This is selectable in the system.cfg file using the USE_COMPACT_FLASH parameter. Recording to CompactFlash requires a special daughter card and enclosure from ICS.
- Fixed a bug in setting up the hardware encoding of ASCB status parameters when in the hardware PDD transmission mode.
- Added the optional USE_STS_LED_FOR_REC_STS parameter to the system configuration file, which allows the bi-color status LED to be used for indicating ASCB recording status rather than the legacy purpose of indicating a valid connection to the FlightLine software.
- Added the optional parameter HW_TX_PDD_ENABLE to the system configuration file. This parameter is synonymous with HW_PDD_ENABLE. Either value can be used. The new parameter was created for clarification because it controls only the hardware PDD transmit modules and not the hardware PDD receive module, which is always enabled.

Note: This software release can only be used with FPGA revisions 04231401 or 05121401.

Release 24-Apr-2014:

Software Revision Numbers
==========

CPU 0: Apr 24 2014 11:16:56
CPU 1: Apr 24 2014 11:17:06

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- Implemented hardware modules for the PDD and PDD API transmit functions to allow automated transmission onto the ASCB bus. The HW_PDD_ENABLE parameter must be set to TRUE in the system.cfg file to enable this functionality. In addition, valid produce ESCAPE (PDD) registries must be programmed into the DataTap-10 via the microSD card and a produce TIS configuration file must exist on the microSD card for each ASCB bus. Refer to the user's manual or system.cfg file for further details.
- Added a dynamic memory allocation scheme based on the detected RAM size such that separate software loads are no longer required. Note that the 4MB or 8MB RAM is necessary in order to use the hardware PDD transmit functionality or the ASCB recording feature.
- Added to the Telnet server screens the displaying of all parameters being produced as well as the registry header information for all programmed ESCAPE registries. Pressing 'r' while on the Parameter Display page or the Initialization Status page allows cycling through each of the three registries (Consume, Produce 0, Produce 1).
- Added an AUTO feature to the system.cfg file for assigning the DataTap-10 NIC IDs using the ASCB0_NIC_IDS and ASCB1_NIC_IDS parameters. AUTO is only valid when HW_PDD_ENABLE is set to TRUE and valid produce ESCAPE registries are loaded, otherwise no ASCB transmission will occur. This feature indicates to the DataTap-10 to assign itself the Host NIC IDs extracted from the two produce ESCAPE registries. Note that if neither extracted NIC ID is that of a timing master and there is no other timing master on the bus, no ASCB transmission will occur. In this case, the DataTap-10 NIC IDs can be manually specified to include a timing master since the DataTap-10 can act as multiple NIC IDs per bus. The extracted Host NIC IDs can be found on the Initialization Status page of the Telnet server.
- Added the following optional parameters to the system configuration file:
  - UDP_LSTN_PORT_SIU0
  - UDP_LSTN_PORT_SIU1
  - HW_PDD_ENABLE
  - USE_COMPACT_FLASH
  - The "AUTO" option for ASCB0_NIC_IDS and ASCB1_NIC_IDS

Note: This software release can only be used with FPGA revision 04231401.

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Releases for FPGA Revision 08301301

Release 19-Mar-2014:

Software Revision Numbers
==========

CPU 0: Mar 19 2014 09:53:25 (4MB Local RAM)
CPU 1: Mar 19 2014 09:53:44 (4MB Local RAM)

CPU 0: Mar 19 2014 09:53:36 (2MB Local RAM)
CPU 1: Mar 19 2014 09:53:47 (2MB Local RAM)

- Changed the method of parsing the NIC registry during transmission to allow PDD registries of individual MAU modules to be used rather than requiring a "produce all" registry set.

Note: This software release can only be used with FPGA revision 08301301.

Release 26-Feb-2014:

Software Revision Numbers
==========

CPU 0: Feb 26 2014 12:33:34 (4MB Local RAM)
CPU 1: Feb 26 2014 12:33:50 (4MB Local RAM)

CPU 0: Feb 26 2014 12:33:43 (2MB Local RAM)
CPU 1: Feb 26 2014 12:33:53 (2MB Local RAM)

- Fixed a bug in the Passthru mode of operation. Passthru does not work in any previous releases for FPGA revision 08301101. The issue has been fixed and verified in this release.
- Added the ability to automatically detect whether a 2MB or 4MB Local RAM is installed and added the result to the Telnet display. For the 2MB versions, ASCB recording is disabled and only 2048 rather than 8192 parameters can be processed for ASCB reception. Note that the software files are different for the 2MB and 4MB versions.

Note: This software release can only be used with FPGA revision 08301301.

Release 11-Nov-2013:

Software Revision Numbers
==========

CPU 0: Nov 11 2013 11:42:15
CPU 1: Nov 11 2013 11:42:28

- Removed the padding bytes which previously forced 32-bit alignment in the raw/full recording files at the start of each frame.
- Removed the padding bytes which previously forced 32-bit alignment in the decoded/partial recording files at the start of each recorded datagram.

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- Bumped the software release number sent in the DIANE headers to 2.

Note: This software release can only be used with FPGA revision 08301301.

Release 10-Sep-2013:

Software Revision Numbers
==========

CPU 0: Sep 10 2013 12:31:17
CPU 1: Sep 10 2013 12:31:23

- Added support for the decoding of ASCB parameters in hardware rather than software.
- Added support for recording ASCB raw and decoded data to the microSD card.
- Added support for sending and recording of DIANE packets.
- Added Precision Time Protocol version 2 support.
- Added displaying of error codes through the bi-color status LED.
- Added support for health and status information via the discrete outputs.
- Added the following optional parameters to the system configuration file:
  - HOST_IP_SYNC
  - UDP_HOST_PORT_SYNC
  - UDP_SYNC_EN_DEF
  - OUTPUT_HEALTH_INFO
  - SD_MEMORY_RECORD_WARNING
  - USE_TIMING_SOURCE
  - PARTIAL_SEND_REC_FORMAT
  - PARTIAL_SEND_[32:1]_RATE
  - PARTIAL_SEND
  - PARTIAL_REC_FILE
  - PARTIAL_REC
  - FULL_SEND_REC_FORMAT
  - FULL_REC_FILE
  - FULL_REC
  - FULL_SEND
  - DEVICE_NUM
  - PTP_ANNOUNCE_TIMEOUT
  - PTP_TIMEZONE_OFFSET

Note: This software release can only be used with FPGA revision 08301301.

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Releases for FPGA Revisions 07241301 and 10301201

Release 9-Sept-2013:

Software Revision Numbers
==========

CPU 0: Sep 9 2015 09:17:14
CPU 1: Sep 9 2015 09:17:29
CPU 2: Sep 9 2015 09:17:33

- Added a software work-around to account for a bug in the IRIG logic. The bug caused the IRIG time to rollover to 00:00:00 from 17:59:59 and to increment to 24:00:00 from 23:59:59. The condition would last for one full second until the next IRIG frame was received and would correct the time. The logic bug was fixed in FPGA revision 09031401.

Note: This software release can only be used with FPGA revisions 07241301 or 10301201.

Release 24-July-2013:

Software Revision Numbers
==========

CPU 0: Jul 24 2013 13:04:05
CPU 1: Jul 24 2013 13:04:20
CPU 2: Jul 24 2013 13:04:23

- No software changes, but revision numbers changed to match firmware release, which adds hardware clearing of NIC receive frame buffers at the start of each ASCB frame.

Note: This software release can only be used with FPGA revisions 07241301 or 10301201.

Release 7-May-2013:

Software Revision Numbers
==========

CPU 0: May 7 2013 14:18:49
CPU 1: May 7 2013 14:19:02
CPU 2: May 7 2013 14:19:05

- Increased the frequency of reading the ADC channels to one channel every 10 milliseconds. The channels are read in order starting at channel 0 and ending at channel 3 before looping back around to channel 0 again.
- Increased the frequency of the UDP status messages being sent out of the DataTap-10. A status message is now sent out once per ASCB frame (12.5 milliseconds) rather than every 100 milliseconds.

Note: This software release can only be used with FPGA revision 10301201.

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Release 2-May-2013:

Software Revision Numbers
==========

CPU 0: May 2 2013 07:08:25
CPU 1: May 2 2013 07:08:40
CPU 2: May 2 2013 07:08:43

- Added the display of the NIC and PDD registry headers to the Telnet pages.
- Added the ability to record ARINC-429 data to the microSD card. Control of the recording is handled through Telnet or UDP command packets.

Note: This software release can only be used with FPGA revision 10301201.

Release 15-Jan-2013:

Software Revision Numbers
==========

CPU 0: Jan 15 2013 10:42:02
CPU 1: Jan 15 2013 10:42:16
CPU 2: Jan 15 2013 10:42:19

- Added additional error checking when decoding ASCB parameters.
- Sped up the PDD registry lookup at initialization time.
- Added a check to ensure the NIC registry prior to enabling ASCB reception.
- Added a check to ensure the PDD registry is valid prior to looking up the parameters listed in the tis.cfg file at initialization time.

Note: This software release can only be used with FPGA revision 10301201.

Release 30-Oct-2012:

Software Revision Numbers
==========

CPU 0: Oct 30 2012 14:23:34
CPU 1: Oct 30 2012 14:23:55
CPU 2: Oct 30 2012 14:23:59

- Added the ability to decode and process Enhanced-ASCB (eASCB).
- Added the ability to indicate a DC offset is present on the IRIG signal based on the IRIG_HAS_DC_OFFSET setting in the system configuration file. A value of AUTO causes the DataTap-10 to automatically alternate between expecting a DC offset and not expecting a DC offset every 3 seconds while not locked onto an IRIG signal.
- Added the following optional parameters to the system configuration file:
  - IRIG_HAS_DC_OFFSET
  - ENHANCED_ASCB_MODE

Note: This software release can only be used with FPGA revision 10301201.

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Update Instructions:

The included "mb*.srd" files must be copied onto the DataTap-10's microSD card. This can be accomplished using the "DT10 Update" feature of FlightLine version 12.1 or later, by manually transferring them via FTP, or by removing the microSD card from the unit and copying them directly onto the card using a PC. A power cycle then initiates the update sequence. The LEDs on the front of the DataTap-10 will flash in a rectangular pattern while the update is taking place. The update takes less than 20 seconds to complete. The files will automatically be deleted from the microSD card by the DataTap-10 once the update has completed successfully. If power is removed while the update is in progress, the update will simply resume when power is re-applied.

Please refer to the DataTap-10 User's Manual for futher details.